CHIPS JOINT UNDERTAKING

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EUROPEAN PARTNERSHIP

WHAT IS CHIPS JOINT UNDERTAKING?

Public-private partnership (PPP)

Partnerships between public authorities and industry intend to bring project results closer to the market and improve the link between research and societal growth. The PPPs are based on long term contracts that can take many different legal forms, from contractual partnerships to specific legal entities.

Joint undertaking (JU)

A Joint Undertaking is an institutionalized PPP with its own legal identity, with its own governance, budget etc.. In most cases, like for the Chips JU, the JUs are established by an EU regulation called the Single Basic Act which defines what the JU has to do and how it must do it. Most of the rules governing the JUs are very similar to those of the European Commission.

Chips JU

Chips JU was established in September, 2023, in an amendment to the Single Basic Act to implement the first pillar of the Chips Act and to continue the activities of its predecessors in the field of electronic components and systems (ECS). The Chips JU is a tri-partite partnership between the EC, the participating states and European industries; most of our actions are funded jointly and equally by these actors.

Chips Act: Entry into force, 21 September 2023

Signatures 13 September, Publication 18 September 2023

Roberta Metsola (European Parliament President)

José Manuel Albares Bueno (Council Presidency)

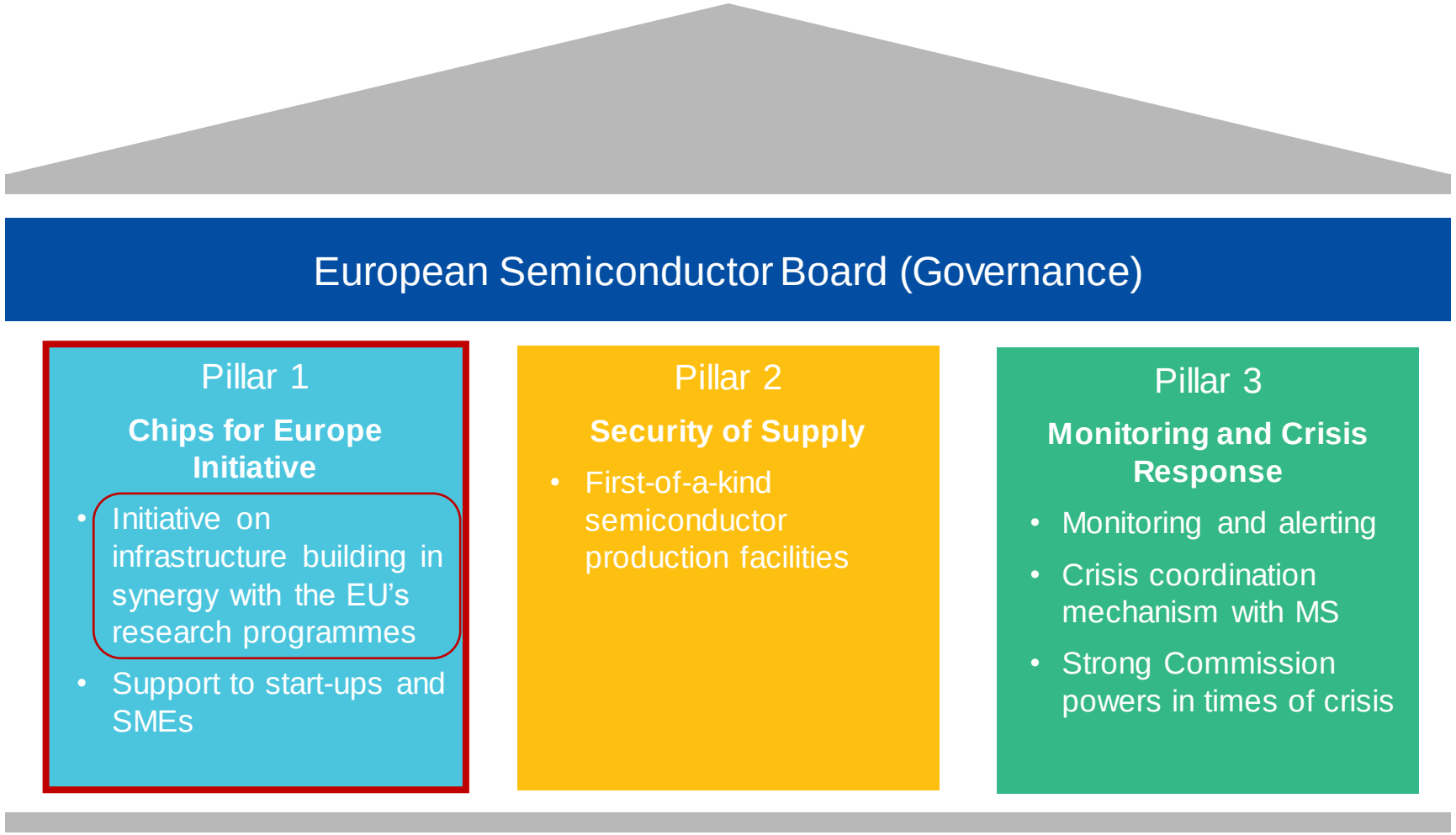
Chips Act:

https://eur-lex.europa.eu/eli/reg/2023/1781/oj

Single Basic Act amendment:

https://eur-lex.europa.eu/eli/reg/2023/1782/oj

THE 3 PILLARS OF THE CHIPS ACT



CHIPS JU AND ITS PREDECESSOR KEY DIGITAL TECHNOLOGIES JU (KDT JU)

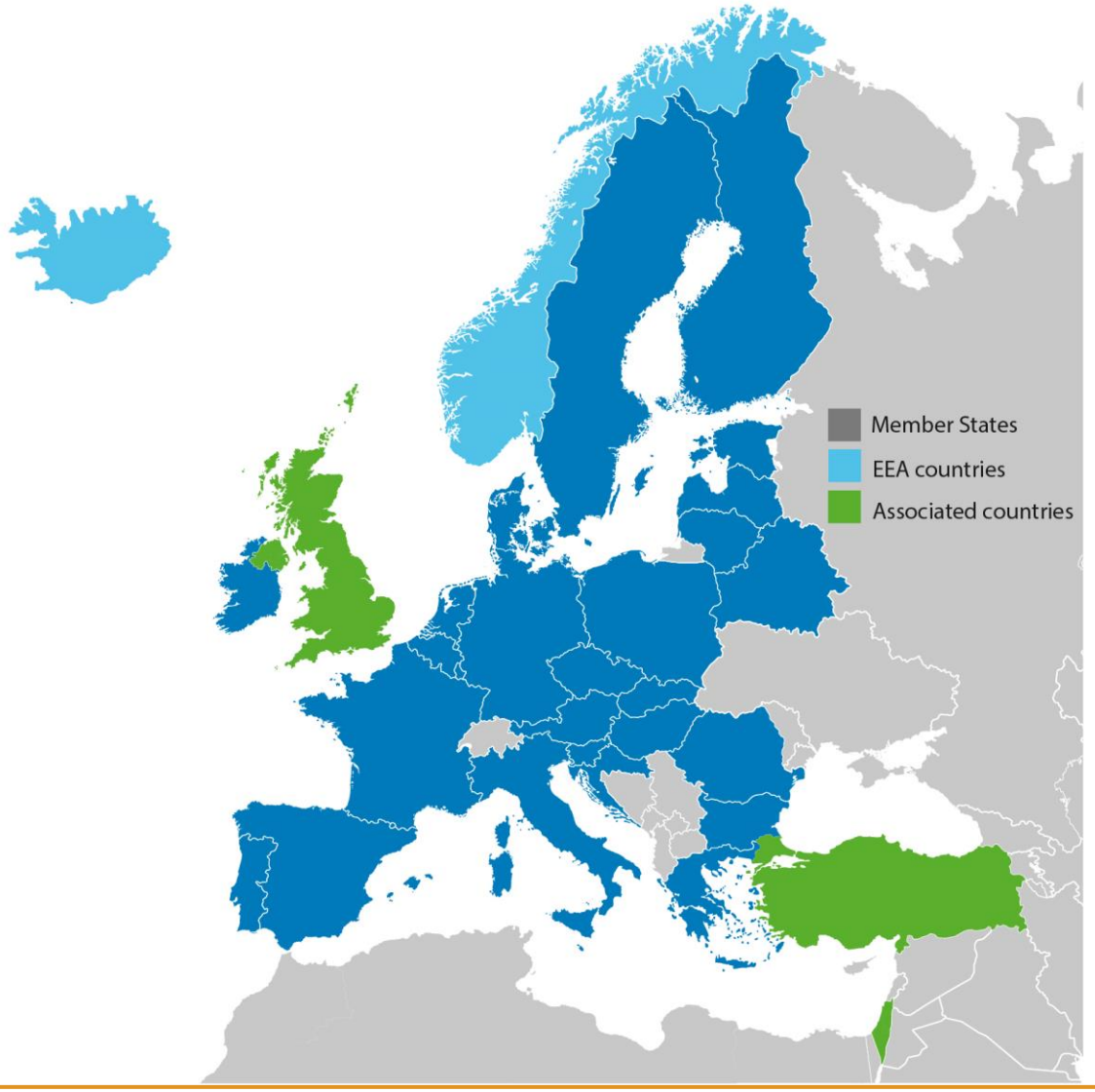
Non-initiative

- **KDT General Objectives**
  - a) Reinforce EU strategic autonomy in electronic components and systems
  - b) Establish EU scientific excellence and innovation leadership
  - c) Ensure that components and systems technologies address Europe's societal and environmental challenges
- **From KDT to Chips JU**

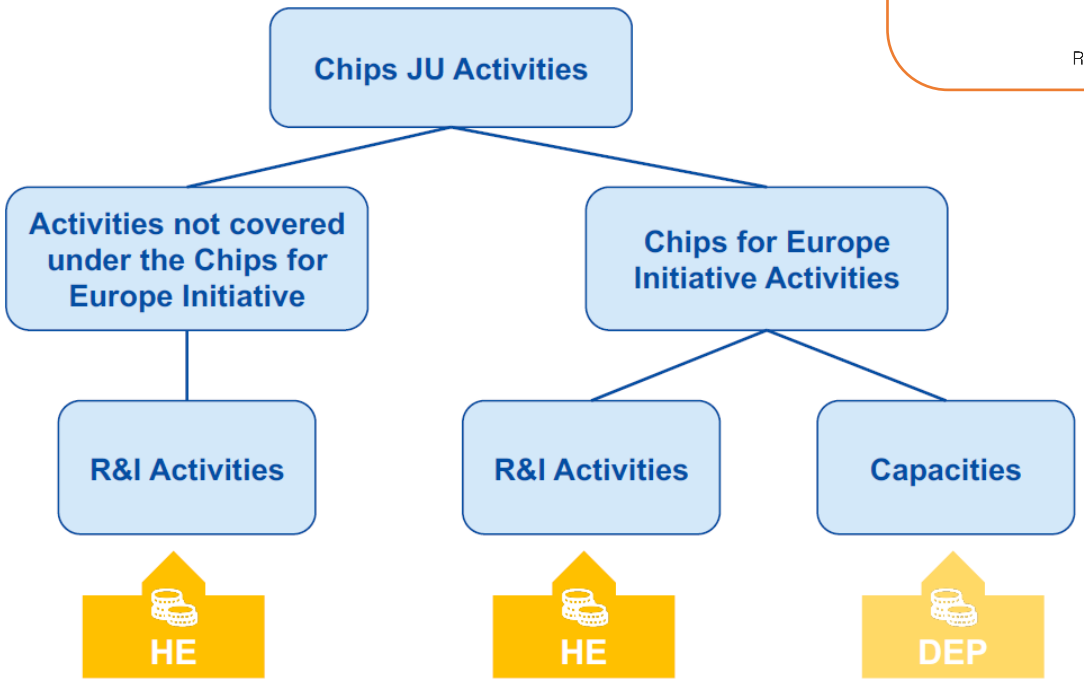
Initiative

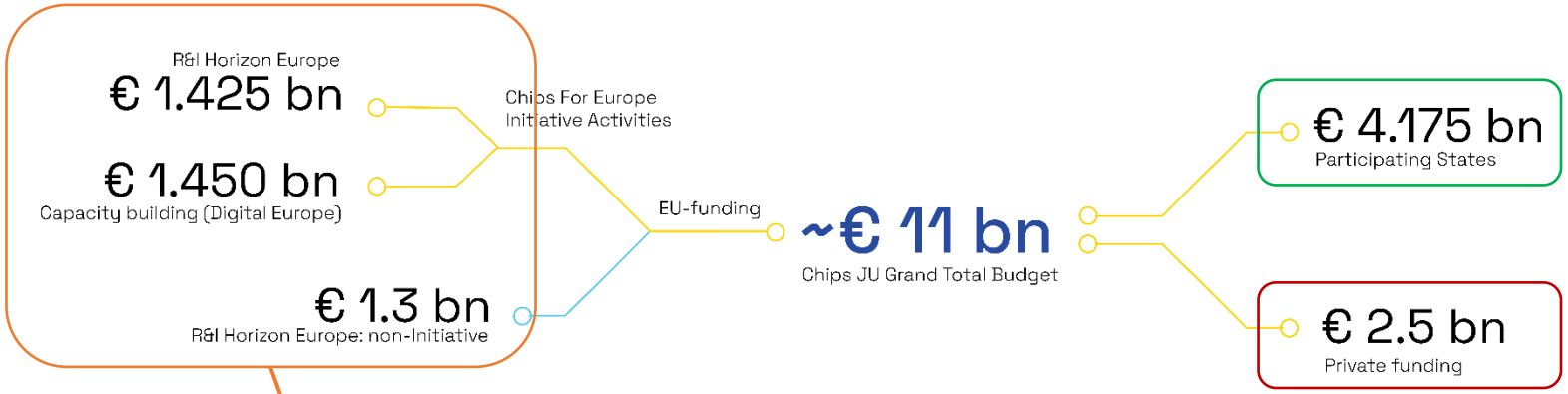
  - d) Pilot lines
  - e) Design platform
  - f) Competence centers
  - g) Quantum chips technology

  Digital Europe Programme in addition to Horizon Europe
- **Disclaimed:** ***we know that the WP2023-2027 will need to be updated/amended in the spring and some details on the following pages may change***
- Link to work programme 2023-2027: https://www.chips-ju.europa.eu/Library-1 (may be updated!)



CHIPS JU

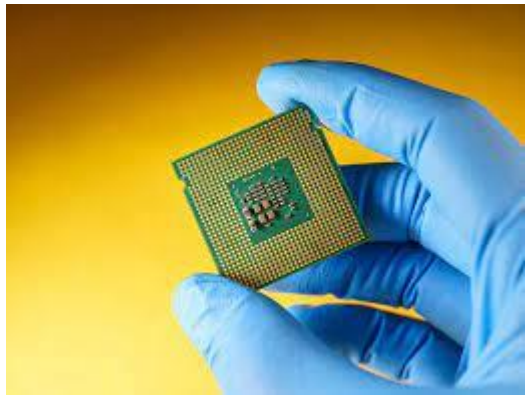




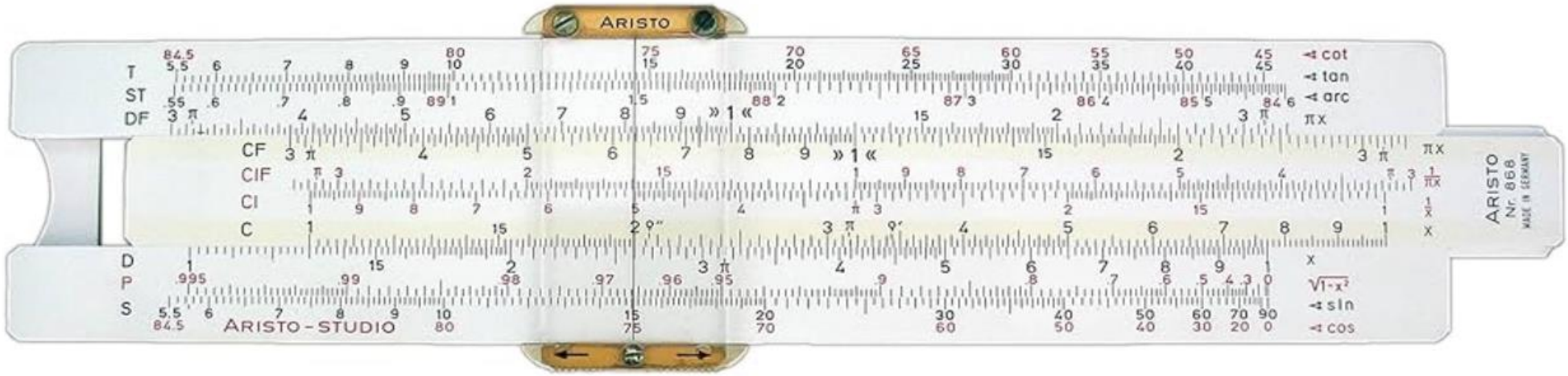
EU Contribution to Chips JU (excl	Chips for Europe Initiative	Non-Initiative	Total
R&I (Horizon Europe)	1.425	1.300	2.725
Cap building (DEP)	1.450	n.a.	1.450
Total	**2.875**	**1.300**	**4.175**

CHIPS AND COMPUTING

Chips



No chips



CHIPS AND COMPUTING: RISC-V

- **ECSEL heritage** - The ECSEL portfolio covers a variety of RISC-V aspects at a **project task level**
  - **Scope: architecture** extensions (e.g., accelerators, co-processors); (Low Power/High Performance) **microarchitectures** (e.g., implementations of the architectures);(Low Power) HW **realizations** (e.g., FD-SOI – By MEANS of?); **SW support** for RISC-V: System SW and tools for design, verification, testing, etc.
  - **ECSEL projects with RISC-V** tasks - **OCEAN 12 (2017-1-IA), CPS4EU (2018-1-IA), VALU3S (2019-2-RIA), FRACTAL (2019-2-SP2), Energy ECS (2020-1-IA), StorAIge (2020-1-IA), DAIS (2020-2-RIA) – most of these have also addressed AI.**

KDT JU/Chips JU RISC-V strategy – focused and linked actions

- Recommendations and **Roadmap for European Sovereignty** in Open Source Hardware, Software, and RISC-V Technologies , 2022
- **SRIA update on RISC-V, 2022**
- **Automotive RISC-V roadmap** - The Road towards a High-Performance Automotive RISC-V Reference Platform , 2023, updated 2024

KDT JU/Chips JU RISC-V calls

- **Call 2021-1-IA-Focus-Topic-1-Development of open sources RISC-V building blocks**
  - **Project TRISTAN, 47 Partners,** *Total cost: € 54,371,711.93; Max HE Funding €15,597,798.00; National Funding: €13,603,678.17*
- **Call 2022-1-IA Topic 3: Focus topic on Design of Customisable and Domain Specific Open-source RISC-V Processors (IA)**
  - **Project ISOLDE, 39 Partners,** *Total cost: €* 39,410,109.71*; Max HE Funding €*11,582,733.37*; National Funding: €* 11.451.467,64

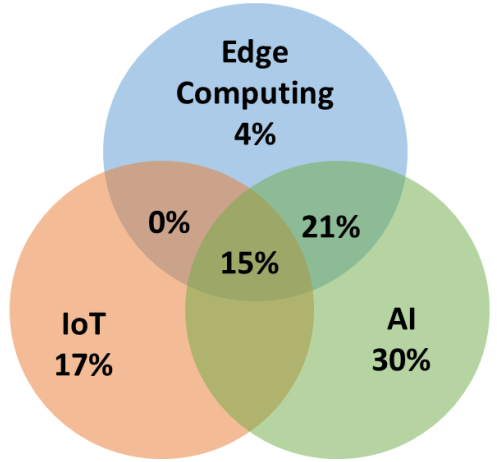
Chips JU investment in RISC-V so far (2 projects contracted):
Total Cost: ***€ 95M***, HE Funding: ***€ 27M***, National Funding: ***€ 25M***, Private in-kind: ***€ 43M***

- **Now Open! Call 2024-1-IA Topic 2: Focus topic on High Performance RISC-V Automotive Processors supporting the vehicle of the future -**
  - **Expected:** *Max 70 partners, Approx. cost: **€ 60-80M**; Max HE Funding **€ 20M**; Max National Funding: **€ 20M***

CHIPS AND COMPUTING: AI

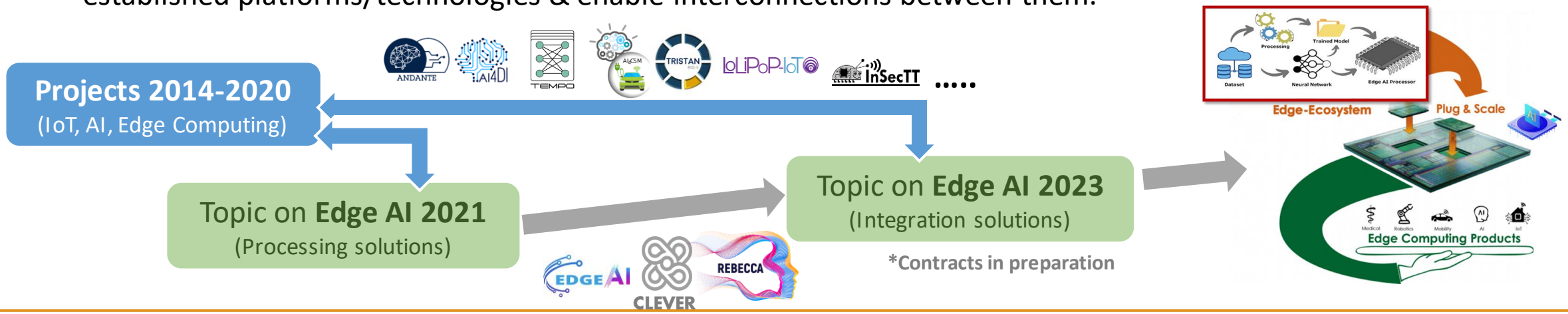
2014-2020. Three key technological areas: AI, IoT and Edge Computing

- 47 out of 92 of our projects (51%) produced results in these areas (2014-2020).
- Results included: algorithms, HW components (e.g., devices, connectivity techs), architectures/platforms, cloud-to-edge techs, contributions to standards and open-source initiatives.
- Mostly for industrial, mobility and energy applications.



2021-2027. Towards a Strong European Edge AI Ecosystem

➢ Projects are expected to incrementally co-create a strong European edge AI ecosystem to strengthen established platforms/technologies & enable interconnections between them.



CHIPS JU: FIRST CALLS OPENED IN DEC. 2023

Call	Topic	Max EU Contribution	Participating States' contribution	Total
Chips-CPL-1	Pilot line on advanced sub 2nm leading-edge system on chip technology	700 MEUR	700 MEUR	1,400 MEUR
Chips-CPL-2	Pilot line on advanced Fully Depleted Silicon On Insulator technologies targeting 7nm	420 MEUR	420 MEUR	840 MEUR
Chips-CPL-3	Pilot line on advanced Packaging and Heterogenous Integration	370 MEUR	370 MEUR	740 MEUR
Chips-CPL-4	Pilot line on advanced semiconductor devices based on Wide Bandgap materials	180 MEUR	180 MEUR	360 MEUR

- Calls closed on February 29, 2024. Complex call starting with a Call for Expression of Interest leading to a Hosting Agreement and a Joint Procurement Agreement, and calls for related HE and DEP grants.
- Expected project start in late 2024.

CHIPS JU: UPCOMING CALLS (NON-INITIATIVE)

Call	Topic	Max EU Contribution
Chips-2024-1-IA Topic 1	Innovation Action on major challenges identified in the Strategic Research and Innovation Agenda (SRIA)	103 MEUR
Chips-2024-1-IA Topic 2	High performance RISC-V automotive processors	20 MEUR
Chips-2024-1-IA Topic 3	Software-defined vehicle	20 MEUR
Chips-2024-2-RIA Topic 1	Research and Innovation Action on major challenges identified in the SRIA	52 MEUR
Chips-2024-2-RIA Topic 2	Sustainable and greener manufacturing	15 MEUR
Chips-2024-3-RIA	Joint call with Korea on heterogeneous integration and neuromorphic computing technologies	6 MEUR

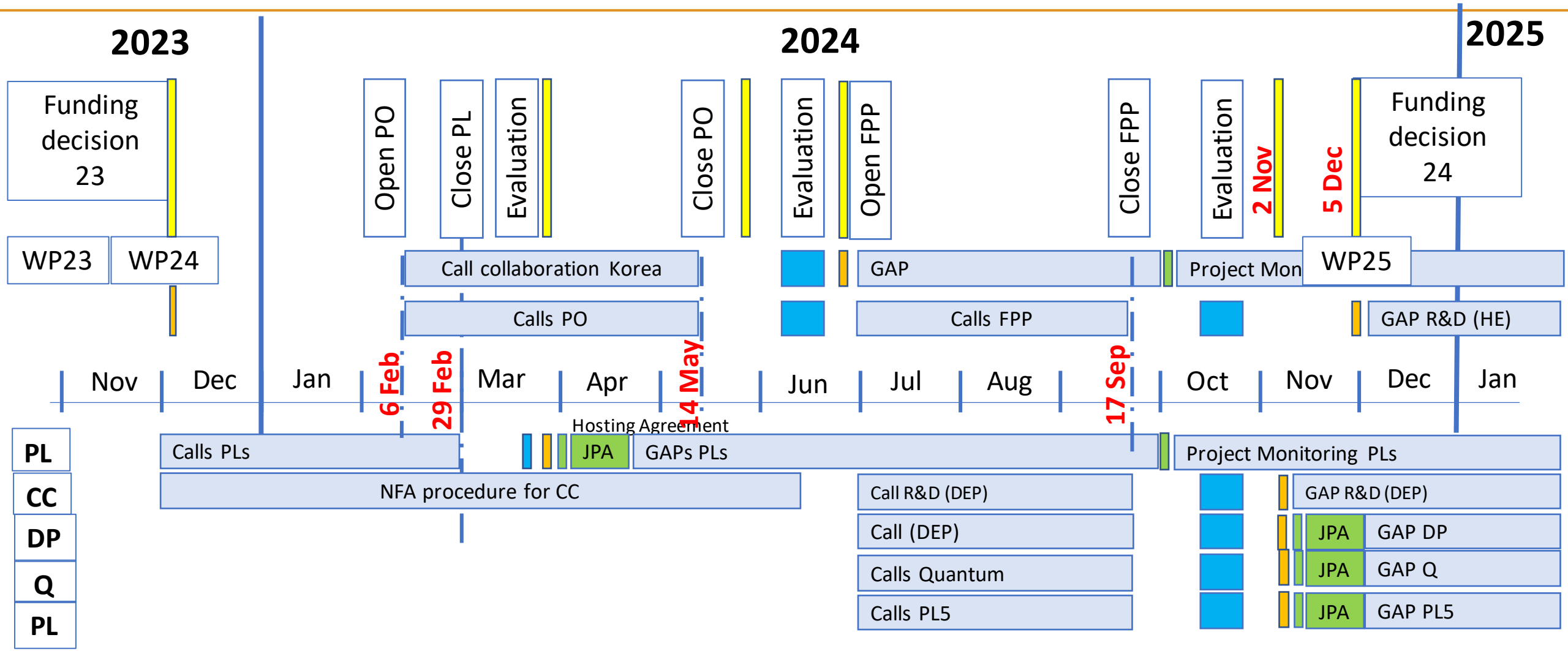
Calls opened on Feb 6, project outlines are due on May 14, and full project proposals on Sept 17, except for the one-stage call with Korea where the deadline for a full proposal is May 14

CHIPS JU: UPCOMING CALLS (INITIATIVE)

Call	Topic	Max EU Contribution
Chips-2024-CDP-1	Design platform. A cloud-based virtual platform that will enable users, particularly academia, start-ups and SMEs, to design and develop their chips. *Details forthcoming.*	330 MEUR
Chips-2024-CPL-5	Additional pilot line(s). *Details forthcoming.*	180 MEUR
Chips-2024-CQC-1	Quantum chips technology (preparatory action for a pilot line)	30 MEUR
Chips-2024-CCC-1	Competence centres. The centres are to provide access to technical expertise and experimentation in the area of semiconductors, helping companies, SMEs in particular, to approach and improve design capabilities and developing skills. Max 1 per EU MS or EEA country, funding up to 1 MEUR/yr from the EU for 4 years, to be matched nationally. Restricted call after national processes.	116 MEUR
Chips-2024-CCC-2	European Network of Chips Competence Centres (CSA)	4 MEUR

Calls will open July 8 and close Sept 17.

SUMMARY OF CALLS 2024



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THANK YOU!