EuroHPC JOINT UNDERTAKING
DECISION OF THE GOVERNING BOARD OF THE EuroHPC JOINT UNDERTAKING No 35/2022
Approving the launch of the call for establishing a Framework Partnership Agreement for developing a large-scale European initiative for High Performance Computing ecosystem based on RISC-V

THE GOVERNING BOARD OF THE EUROHPC JOINT UNDERTAKING,

Having regard to Council Regulation (EU) 2021/1173 of 13 July 2021 on establishing the European High Performance Computing Joint Undertaking and repealing Regulation (EU) 2018/1488[1] (hereinafter, "the Regulation"),

Having regard to the Statutes of the European High Performance Computing Joint Undertaking annexed to the Regulation (hereinafter the "Statutes") and in particular to Articles 1(i) and 7.5(c) thereof,

Having regard to the Governing Board Decision No 41/2022, of 5 December 2022, amending the EuroHPC Joint Undertaking's Work Plan and Budget for the year 2022 (Amendment No. 5),

WHEREAS

(1) The Work Plan 2022 was amended by means of Governing Board Decision 41/2022, of 5 December 2022.

(2) The Governing Board should approve the launch of Calls for Proposals, in accordance with the annual work plan.

(3) The Executive Director of the EuroHPC Joint Undertaking should manage the calls for proposals as provided for in the annual work plan and administer the grant agreements and decisions;

HAS ADOPTED THIS DECISION:

[1] *OJ L 256, 19.7.2021, p. 3–51*

Article 1

The Governing Board hereby approves the launch of call for establishing a Framework Partnership Agreement for developing a large-scale European initiative for High Performance Computing ecosystem based on RISC-V, in accordance with the annual Work Plan of the EuroHPC Joint Undertaking for the year 2022, as approved by Governing Board Decision No 41/2022, of 5 December 2022.

Article 2

The Executive Director of the EuroHPC Joint Undertaking is hereby instructed to launch the EuroHPC call for establishing a Framework Partnership Agreement for developing a large-scale European initiative for High Performance Computing ecosystem based on RISC-V, further to the adoption of and in accordance with the annual Work Plan of the EuroHPC Joint Undertaking for the year 2022, as approved by Governing Board Decision No 41/2022, of 5 December 2022.

The call on EuroHPC Application Support Service shall be published at least:

- on the website of the EuroHPC Joint Undertaking;
- on the Horizon Europe single portal for participants (Funding and Tenders Opportunity Portal).

Article 3

This Decision shall enter into force on the date of its adoption.

Done at Luxembourg, on 6 December 2022

For the Governing Board

[e-signed]

Herbert Zeisel

The Chair

Annex I: Call for establishing a Framework Partnership Agreement for developing a large-scale European initiative for High Performance Computing ecosystem based on RISC-V.

Annex I

Call for establishing a Framework Partnership Agreement for developing a large-scale European initiative for High Performance Computing ecosystem based on RISC-V

TECHNOLOGY – RESEARCH AND INNOVATION (R&I)

The European Chips Act identified RISC-V as one of the next-generation technology where Europe should invest in order to preserve and strengthen its leadership in research and innovation as well as in equipment manufacturing, contributing to build and reinforce the Union's own capacity to innovate in the design, manufacturing and packaging of advanced, energy-efficient and secure chips, and turn them into manufactured products. This spans from micro-controllers up to high-end chips needed for data centres and supercomputers. Early on the technology development should be tied to big industrial use cases to make sure the development addresses a broader European market and contributes to the digital sovereignty beyond scientific HPC. These developments do not only target the state-driven supercomputer-market but also broader, industry-driven markets.[2]

The RISC-V technology is a credible energy-efficient alternative to the proprietary solutions for processors and accelerators across the computing continuum that are produced outside the EU. The report "*Recommendations and Roadmap for European Sovereignty in Open Source Hardware, Software, and RISC-V Technologies*"[3] elaborated for the Commission by an expert group identified the relevant activities in RISC-V to achieve the above mentioned objectives. It includes High Performance Computing as an application domain for the high-end chips.

The vision of the EuroHPC technology pillar is to develop European critical energy-efficient exascale and post-exascale technologies, architectures and systems technology and their integration in pilot systems, complemented with the deployment of world-class competitive exascale and post-exascale supercomputers based on this technology. This vision is fully in line with the EuroHPC JU regulation's objective of establishing an effective link between technology supply, co-design with users, and future actions involving joint procurement of world-class systems, in order to create a world-class ecosystem in HPC technologies and applications across Europe. This vision should be implemented by a long-term partnership in two steps: one supporting the necessary R&I for technology development, test and integration; followed by an ambitious action for building and deploying the exascale and post-exascale supercomputers based on this technology.

These activities are aligned and complementary to the other activities to be carried out by the KDT/Chips JU and will leverage and contribute to the common work to establish a rich RISC-V ecosystem in Europe. The results of the RISC-V activities supported by the EuroHPC JU are expected to hugely contribute to this ecosystem, in particular for other key sectors using high-end elements such as data centres. The KDT/Chips JU is expected to develop the other vertical sectors besides the high end chips and address the horizontal foundational activities underpinning the development of the full RISC-V ecosystem in Europe.

[2] Citation from MASP 2021, page 19

[3] https://digital-strategy.ec.europa.eu/en/library/recommendations-and-roadmap-european-sovereignty-open-source-hardware-software-and-risc-v

Framework Partnership Agreement (FPA) for developing a large-scale European initiative for High Performance Computing (HPC) ecosystem based on RISC-V

Scope: the aim is to support a Framework Partnership Agreement (FPA) establishing a stable and structured long term partnership between the EuroHPC JU and a consortium of industry, research organisations and the institutions in High Performance Computing who commit themselves to establishing, coordinating and implementing a strategic and ambitious R&I initiative contributing to the development of innovative HPC hardware and software technology based on the open RISC-V ecosystem, followed by an ambitious action for building and deploying the exascale and post-exascale supercomputers based on this technology.

This partnership will be set up through one single FPA, which will ensure the implementation of the initiative through several complementary parallel and consecutive Specific Grant Agreements (SGAs) that will carry out the different activities in a common framework. The SGAs will be implemented as Research and Innovation Actions (RIA) or Innovation Actions (IA) in function of the concrete objectives of the action. The FPA should be carried out in different phases, which will be triggered after the attainment of appropriate intermediate progress milestones identified by the Consortium. The FPA will permit the coordinated development of the technology, its validation and the nurturing of the ecosystem. The developments should be integrated in at least one pilot demonstrator to validate the developments and demonstrate the scalability potential towards exascale systems. The demonstrator should be installed in a pre-operational environment in European supercomputing centres for user testing and validation. The FPA and its SGAs should target delivering of technological components for building and deploying in the EU exascale and post-exascale supercomputers based on European technology.

The FPA is expected to pursue an inclusive approach in the development of the necessary EU-wide RISC V ecosystem, ensuring European wide participation of relevant stakeholders across the EU and take-up of the technology developed. The FPA should include supercomputing centres, research institutes, universities, RTOs, industry, SMEs as well as any other organisations that can play a role in the realisation of the objectives of the initiative. The participation of the leading supercomputing centres in Europe is essential to provide upfront the general specifications of the future European supercomputers to ensure the proper alignment of the technological developments to the needs of the users. In addition, the FPA should aim towards a strong participation of the European HPC supplier as well as server/cloud supplier industry, including SMEs, so that they can leverage on existing technological developments and activities and, reinforce their capabilities of becoming leading technology suppliers.

The FPA should ensure a common framework for implementation by maintaining a long-term roadmap with a critical timeline and milestones of the necessary activities (including also other related activities funded outside EuroHPC) that would be needed to build and deploy exascale and post-exascale systems in Europe using the technology developed in this initiative.

Proposals for FPAs should present an overall view of the different main areas of work to be implemented by SGAs, addressing them in a co-design approach. The co-design approach should bridge the gap between suppliers and users; define the characteristics and technical features of the new hardware architectures and where necessary the additional key components, existing or to be developed; as well as better computational methods and algorithms adapted to future real HPC application needs with a minimum significative number of use cases that demonstrate the capability of the developed solutions for solving concrete and challenging computational problems demonstrating a competitive

edge in application areas that are crucial for the Union. The FPA should address in a co-design approach at least the topics listed below:

1) RISC-V hardware: addressing the design, development, testing, tape-out of different generations of energy efficient high-end processors and/or accelerators, in particular chiplet-based approaches, for High Performance Computing (HPC), also linked to cloud or data server use cases, using synergies with designs and components developed by projects funded through the Key Digital Technologies Joint Undertaking resp. Chips Joint Undertaking where relevant,
2) integration in test-beds and at least one pilot in pre-operational environments in supercomputing centres for user testing and validation.
3) RISC-V software: develop the full SW stack and the associated software ecosystem for the developed processors and/or accelerators, addressing the system, middleware and application layers. The development should be driven by the needs of relevant HPC workflows and application requirements and cloud or data server use cases where relevant.
4) Develop and/or adapt the other necessary technologies for the integration of the RISC-V based components into industrial grade HPC solutions.
5) Identify the most critical HPC applications and domains and work towards porting and optimising them for the new RISC-V based environment, and the wide take-up of the developed technology by users.
6) Explore and exploit existing manufacturing capabilities in Europe, including existing or under development pilot lines, to fabricate the required components.

The FPA should develop mechanisms guaranteeing that all IP generated in the initiative stays in the EU and will not be transferred to third countries, dedicating an appropriate effort to IP management, protection and exploitation (i.e., IP licensing, IP warranty, etc.).

The FPA should present a professional project structure management, a strategic R&I roadmap to implement the activities, and governance that are appropriate to coordinate the implementation of the future SGAs, including addressing the industrial use cases, and to deliver effectively and efficiently the main results of the initiative. The FPA should put in place appropriate management and progress control mechanisms, in particular, the establishment of common milestones for the SGAs and an intermediate main assessment point to assess the correct advancement of the different work lines towards the goals of the overall initiative.

The FPA should establish interaction with the relevant stakeholders and Programs of the KDT/Chips JU to coordinate work on horizontal issues common to both communities and exploit synergies where relevant, in particular for pilot lines for high end components, common design rules and tools.

Expected Outcome: Framework Programme Agreement (FPA) for European exascale- and post-exascale hardware and software technologies, based on RISC-V in order to deliver high-end processors and/or accelerators and systems based on a strategic research roadmap, and the realisation of test-beds, pilots and/or demonstrators, integrating these processors.

The FPA is expected to address the following outcomes:

- Contribution towards European technological sovereignty, by establishing, maintaining and implementing a strategic R&I roadmap that fosters the European capabilities to design, develop and produce the IP related to high-end processors and/or accelerators based on RISC-V, driven by relevant key performance indicators.
- Designing and delivering energy efficient high-end processors and accelerators for HPC based on RISC-V hardware solutions, test-beds, and at least one pilot integrating these processors/accelerators. The development of European processors and/or accelerators should prepare the technology for its future integration in post-exascale supercomputers to be acquired at a later stage by the EuroHPC JU targeting systems incorporating European technologies.

- A suitable software stack, including key elements such as programming models and runtimes (e.g. languages, compilers, programming environments, communication), libraries (e.g. mathematical, data analytics, AI frameworks), tools (e.g. debuggers, performance, system monitoring), operating system components (e.g. schedulers, workflows, software management, security), and other elements (e.g. for networking, software deployment, system-level composability and modularity of software, etc.).
- The necessary components adapted for the integration of the RISC-V based components in industrial grade HPC or Cloud solutions.
- A selected set of critical HPC applications, encompassing amongst others the mayor EuroHPC use-cases, ported and optimised to the new RISC-V based environment, based on a co-design approach.
- Standards and interface specifications for the software and hardware stack, with clear definition of standardization and licensing schemes of the developed Intellectual Property (IP), with mechanism to guarantee that this IP remains in the EU.
- Reinforce the use of pilot lines based in Europe and, widen the skill base for the design and manufacturing of high-end components.
- A long-term roadmap with a critical timeline, milestones and all the necessary activities that would be needed to build and deploy post-exascale systems in Europe using European technology.

Specific conditions	
Expected EuroHPC JU contribution	The EuroHPC JU estimates that an EU contribution of EUR 135 million matched by the Participating States with a similar amount would allow these outcomes to be addressed appropriately. Only one proposal is expected to be retained. The expected duration of this action is 6 years.
Type of Action	Framework Programme Agreement (FPA)
Call opening	16/12/2022
Call closing	31/3/2023
Eligibility conditions	The conditions are described in General Annex B. The following exceptions apply: In order to achieve the expected outcomes, and safeguard the Union's strategic assets, interests, autonomy, or security, participation is limited to legal entities established in Member States and in the following Associated Countries to Horizon Europe: Iceland, Norway. Proposals including entities established in countries outside this scope specified in the topic/call/action will be ineligible. For the duly justified and exceptional reasons listed in the paragraph above, in order to guarantee the protection of the strategic interests of the Union and its Member States, legal entities established in a Member State or in Iceland and Norway, that are directly or indirectly controlled by third countries that are not OECD countries or by legal entities of third countries that are not OECD countries are not eligible to participate.